



MIDTERM EXAMINATION
SEMESTER SPRING 2005
CS302-Digital Logic Design (S1)

Total Marks:50
Duration:60 Min

Student ID / Login ID	
Name	
PVC Name / Code	
Date	

Maximum Time Allowed: (1 Hour)

Please read the following instructions carefully before attempting any of the questions:

1. Attempt all questions.
2. Calculators are **NOT** allowed.
3. Do not ask any questions about the contents of this examination from anyone.
 - a. If you think that there is something wrong with any of the questions, attempt it to the best of your understanding.
 - b. If you believe that some essential piece of information is missing, make an appropriate assumption and use it to solve the problem.

4. **Circuit Diagrams**, **Equations** and **Truth Tables** should be clear.

Write down all the steps in Subjective Questions. Marks will be deducted for missing steps.

****WARNING: Please note that Virtual University takes serious note of unfair means. Anyone found involved in cheating will get an `F` grade in this course.**

For Teacher's use Only						
Question	Q1	Q2	Q3	Q4	Q5	Total
Marks						

Question No: 1

Marks: : 2+2+2+2+2=10

Select the best possible choice.

a) A NOR's gate output is HIGH if

- I. all inputs are HIGH
- II. any input is HIGH
- III. any input is LOW
- IV. all inputs are LOW

b) A demultiplexer has

- I. one input and several outputs
- II. one input and one output
- III. several inputs and several outputs
- IV. several inputs and one output

c) The difference of 111 - 001 equals

- I. 100
- II. 111
- III. 001
- IV. 110

d) To implement the expression $\overline{A}BCD + A\overline{B}CD + ABC\overline{D}$, it takes one OR gate and

- I. three AND gates and three inverters
- II. three AND gates and four inverters
- III. three AND gates
- IV. one AND gate

e) Which gate is best used as a basic comparator?

- I. NOR
- II. OR
- III. exclusive-OR
- IV. AND

Question No: 2

Marks: 10

Convert $(-7A)_{16}$ into Binary number system and then take 2's complement of the resultant binary number. (Show all necessary steps.)

Question No: 3

Marks: 10

Implement a logic circuit for the truth table given below:

INPUTS			OUTPUTS
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Question No: 4

Marks:6+4=10

a) Draw a 4-variable K-map and label each cell according to its binary value .

(Hint) for 2 -variable k-map

A\B	0	1
0	00	01
1	10	11

b) Expand each expression to standard SOP form.

$$\overline{A}\overline{B}\overline{C}\overline{D} + A\overline{C}\overline{D} + \overline{B}\overline{C}\overline{D} + \overline{A}B\overline{C}\overline{D}$$

Question No: 5

Marks: 4+6=10

Draw a truth table and circuit diagram of 4 bit parallel adder?