

	FINALTERM EXAMINATION FALL 2006 CS302 - DIGITAL LOGIC DESIGN (Session - 2)	Marks: 60 Time: 120min
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StudentID/LoginID: _____

Student Name: _____

Center Name/Code: _____

Exam Date: Tuesday, February 13, 2007

Please read the following instructions carefully before attempting any of the questions:

1. Attempt all questions.
2. Calculators are **NOT** allowed.
3. Do not ask any questions about the contents of this examination from anyone.
 - a. If you think that there is something wrong with any of the questions, attempt it to the best of your understanding.
 - b. If you believe that some essential piece of information is missing, make an appropriate assumption and use it to solve the problem.
4. **Circuit Diagrams, Equations and Truth Tables** should be clear.

For Teacher's use only											
Question	1	2	3	4	5	6	7	8	9	10	Total
Marks											

Question No: 1 (Marks: 2) - Please choose one

The OR gate performs Boolean _____.

- ▶ multiplication
- ▶ subtraction
- ▶ division

- ▶ addition

Question No: 2 (Marks: 2) - Please choose one

How many states does a modulus-4 counter have?

- ▶ 1
- ▶ 2
- ▶ 4
- ▶ 16

Question No: 3 (Marks: 2) - Please choose one

How will a serial in/serial out shift register accept data serially?

- ▶ one bit at a time
- ▶ 8 bits at a time
- ▶ only after a load pulse
- ▶ only after being cleared

Question No: 4 (Marks: 2) - Please choose one

If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be

- ▶ set
- ▶ reset
- ▶ invalid
- ▶ clear

Question No: 5 (Marks: 2) - Please choose one

The storage cell in SRAM is

- ▶ a flip-flop
- ▶ a capacitor
- ▶ a fuse
- ▶ a magnetic domain

Question No: 6 (Marks: 5)

Convert the following POS expression to minimum SOP expression using K-Map

$$(\bar{A} + B)(\bar{A} + \bar{B} + \bar{C})(B + \bar{C} + D)(A + \bar{B} + C + \bar{D})$$

Question No: 7 (Marks: 5)

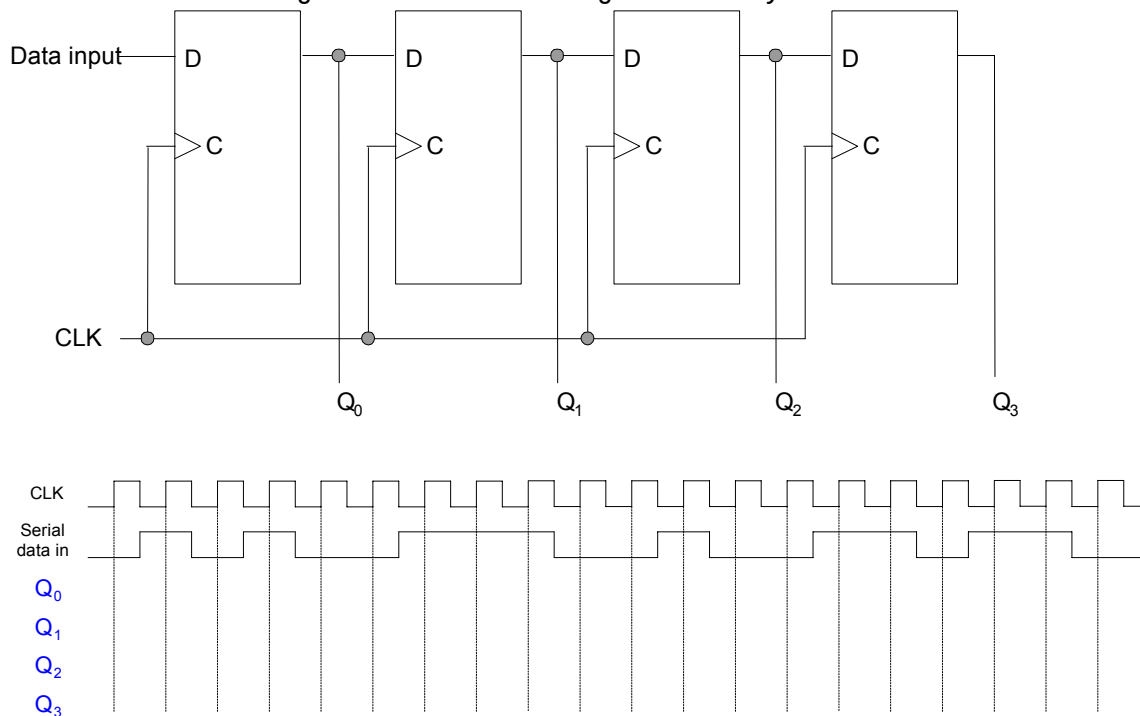
Draw the circuit diagram of the 4x1 Multiplexer.

Question No: 8 (Marks: 20)

Design a 2-bit count-down counter. This is a sequential circuit with two flip flops and one input x. when x=0 the state of flip flop doesn't change. When x=1 the state sequence is 11, 10, 01, 00, 11 and repeat.

Question No: 9 (Marks: 10)

Show a complete timing diagram showing the parallel outputs for the shift register in figure. Use the waveforms in figure below with the register initially clear.



Question No: 10 (Marks: 10)

Draw block diagram of 4-bit Johnson Counter?